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研究獎學金

Research Scholarship

利用缺陷工程應用於無接面多晶鍺錫化合物薄膜電晶體改善I_{ON}/I_{OFF}比例及載子遷移率

Poly-GeSn Junctionless P-TFTs Featuring a Record High I_{ON}/I_{OFF} Ratio and Hole Mobility by Defect Engineering

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研究重點

2-Stage defect engineering of poly-GeSn (Sn: ~5.1%) film for bottom-gate junctionless P-channel thin film transistors (JL P-TFTs), including gas annealing and plasma treatment, is investigated in this work. Stage I of the Ar gas annealing is effective in enhancing the grain size, which helps suppress the grain boundary density and bulk trap density of the surface part of the poly-GeSn film. With the subsequent stage II of the NH_3 plasma treatment, both the defect density at the gate dielectric interface and in the bulk poly-GeSn film can be greatly reduced by terminating the intra- and inter-grain dangling bonds via radical diffusion along the grain boundaries. With the improved defect density of 9.2×10^{11} cm^{-2} by stage I and II, JL P-TFTs exhibit a record high peak field-effect hole mobility of 162.2 cm^2/Vs and an I_{ON}/I_{OFF} ratio of 2.8×10^5 even with a planar structure. In addition, enhanced reliability performance in terms of reduced stress induced leakage current and improved bias induced instability is also achieved. Moreover, the low-thermal-budget process of 500 ^oC for 30 s paves a new avenue towards creating high-performance monolithic 3D ICs.

研究成果

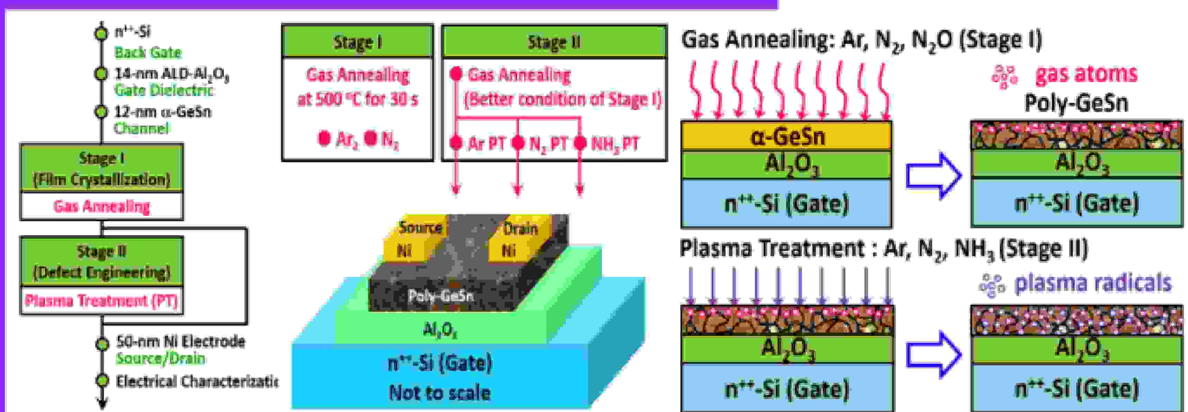

Fig. 1. (a) Process flow of high-performance poly-GeSn JL P-TFTs with 2-stage defect engineering. (b) A schematic diagram of defect engineering for gas annealing (stage I) and plasma treatment (stage II)

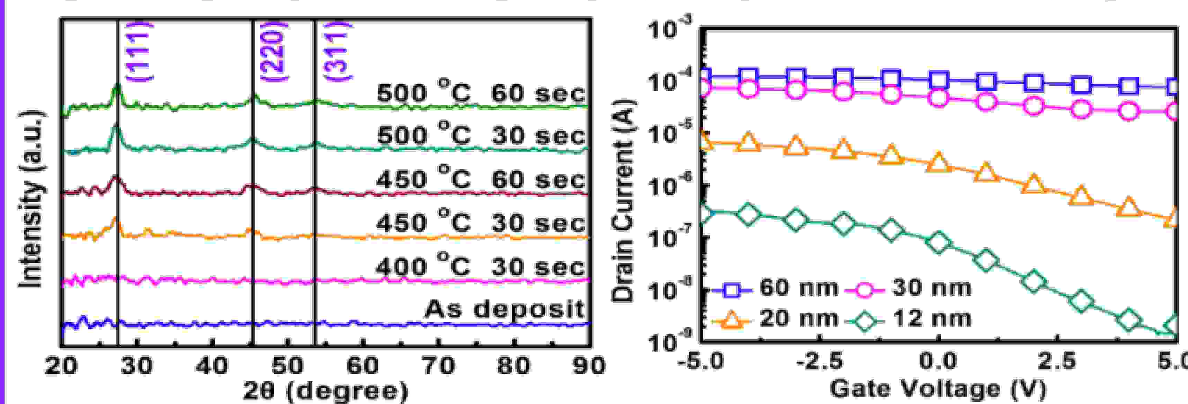

Fig. 2. (a) XRD patterns of poly-GeSn film annealed with different temperature and time in N_2 ambient. (b) I_D-V_G transfer curves for devices with poly-GeSn film of various thicknesses for V_D at −0.05 V.

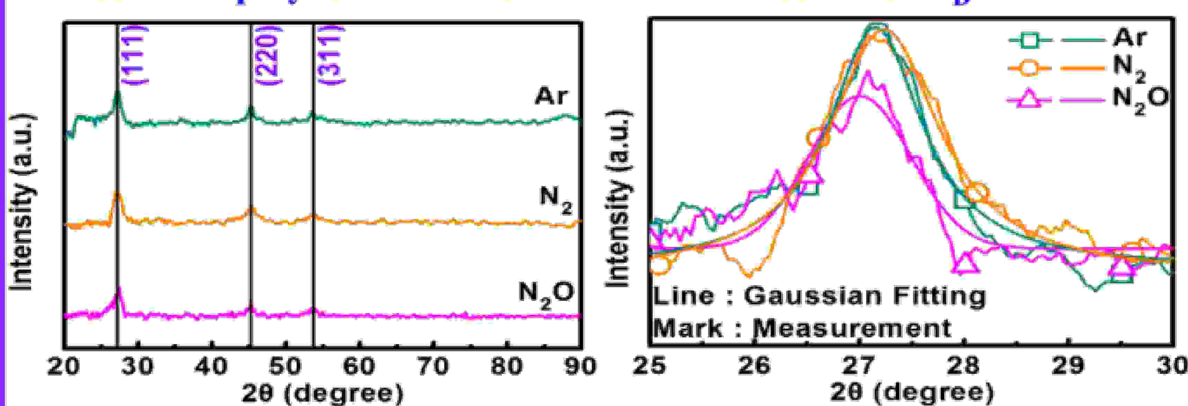

Fig. 3. (a) XRD patterns for poly-GeSn film and (b) enlarged pattern between 25° and 30° with Ar-, N_2- and N_2O-annealed ambient at 500 ^oC for 30 sec.

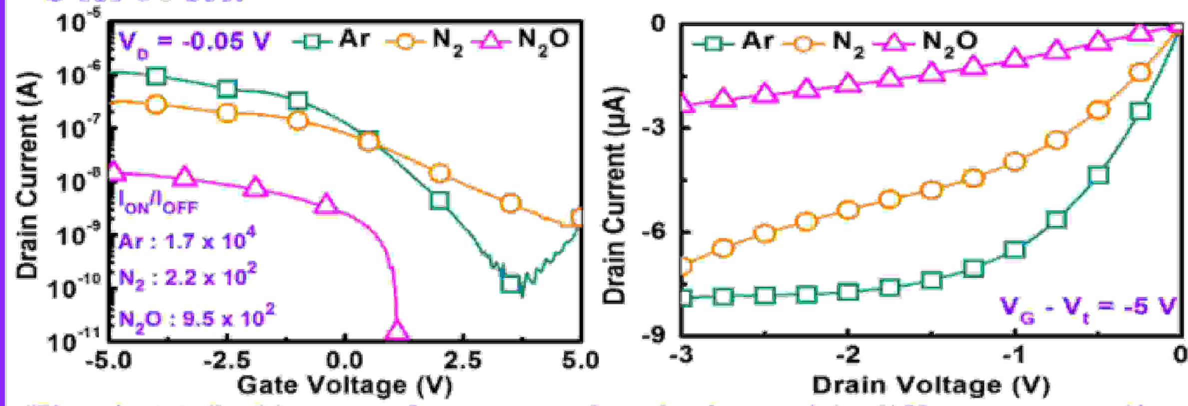

Fig. 4. (a) I_D–V_G transfer curves for devices with different annealing ambient for V_D biased at −0.05 V (b) I_D–V_D output curves for devices with different annealing ambient and biased at V_G-V_t of −5 V.

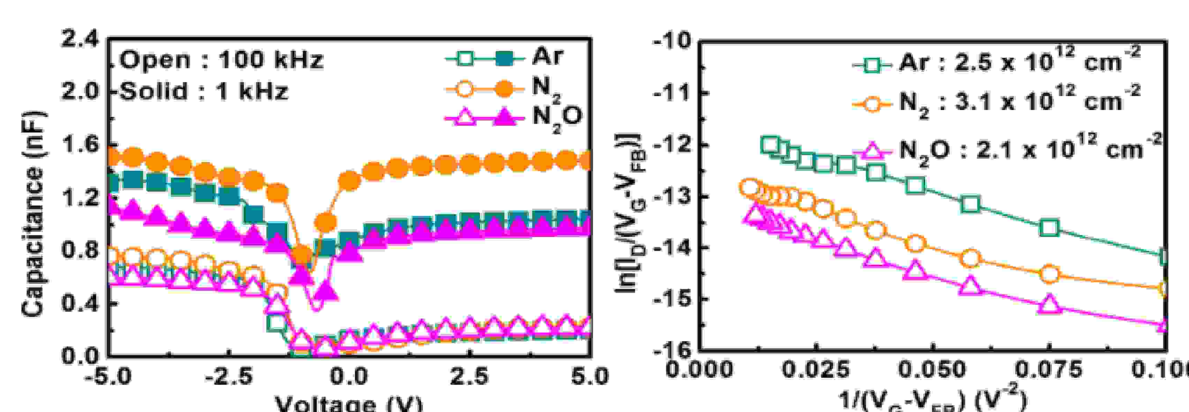

Fig. 5. (a) Capacitance versus voltage for devices with various annealing ambient at 1 and 100 kHz. (b) $\ln[I_D/(V_G-V_{FB})]$ versus $1/(V_G-V_{FB})^2$ for Ar-, N_2- and N_2O-annealed devices for N_{bulk} extraction.

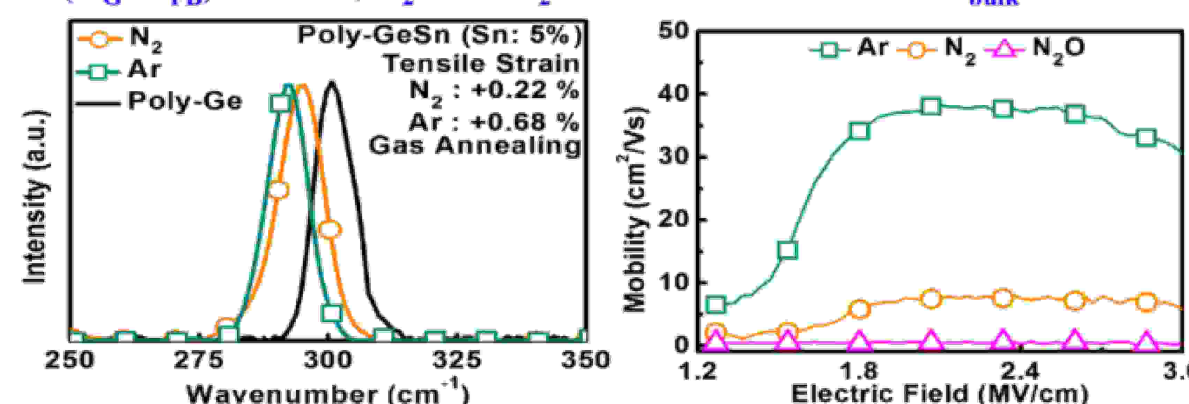

Fig. 6. (a) Raman spectra from GeSn film annealed by N_2 and Ar gas. The spectrum of bulk Ge is also shown for reference. (b) Field-effect hole mobility for devices with various annealing ambient.

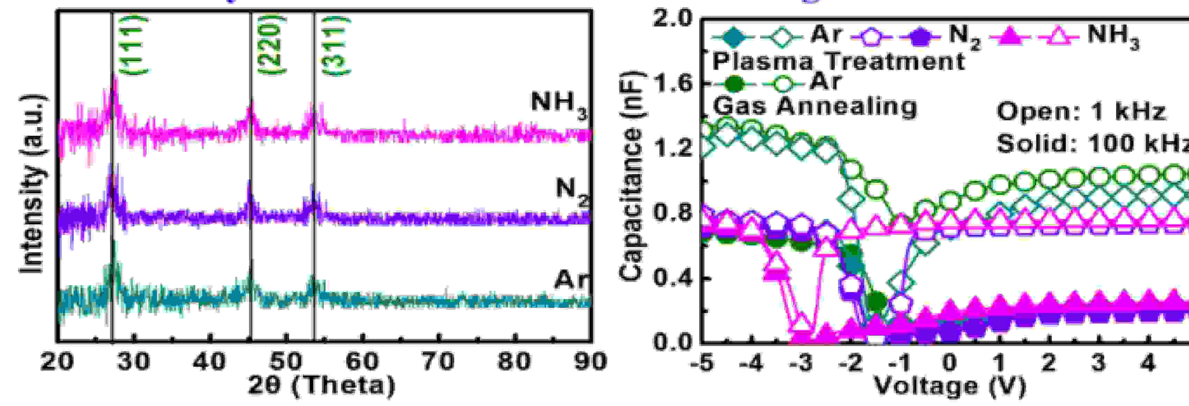

Fig. 7. (a) XRD patterns for GeSn film annealed by Ar gas with additional plasma treatment. (b) Capacitance for devices with Ar, N_2 and NH_3 plasma treatments.

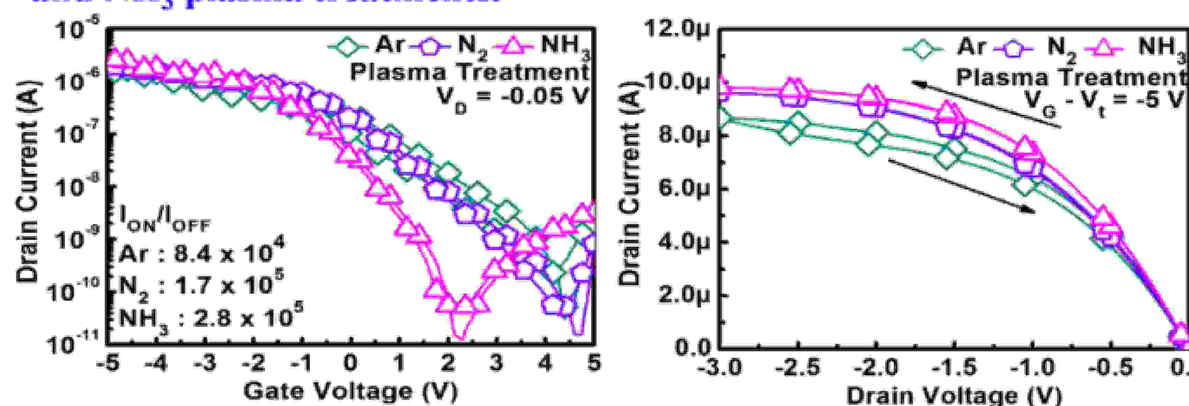

Fig. 8. (a) I_D–V_G transfer curves for Ar-gas-annealed devices with additional plasma treatments. (b) I_D–V_D output curves for devices with different plasma treatments under the same overdrive voltage.

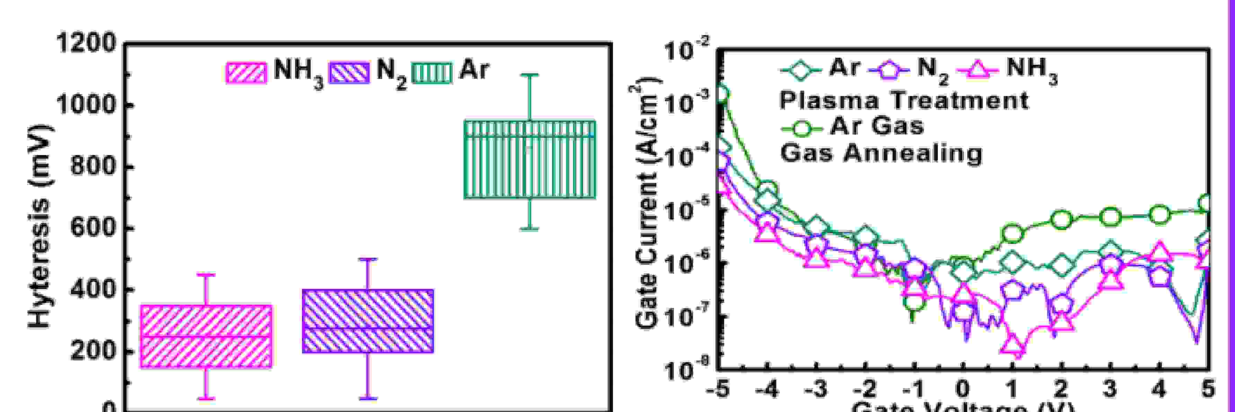

Fig. 9. (a) I_D–V_G hysteresis for 10 devices with various plasma treatments. (b) Gate current for Ar-gas-annealed devices with additional plasma treatments.

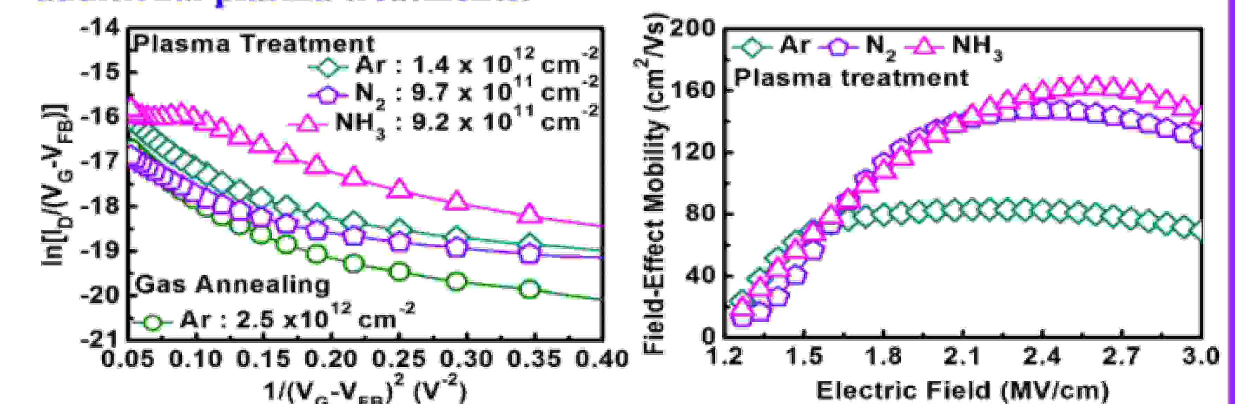

Fig. 10. (a) $\ln[I_D/(V_G-V_{FB})]$ vs. $1/(V_G-V_{FB})^2$ for Ar-gas annealed devices with additional plasma treatments for N_{bulk} extraction. (b) Field-effect hole mobility vs. E-field for devices with various plasma treatments.

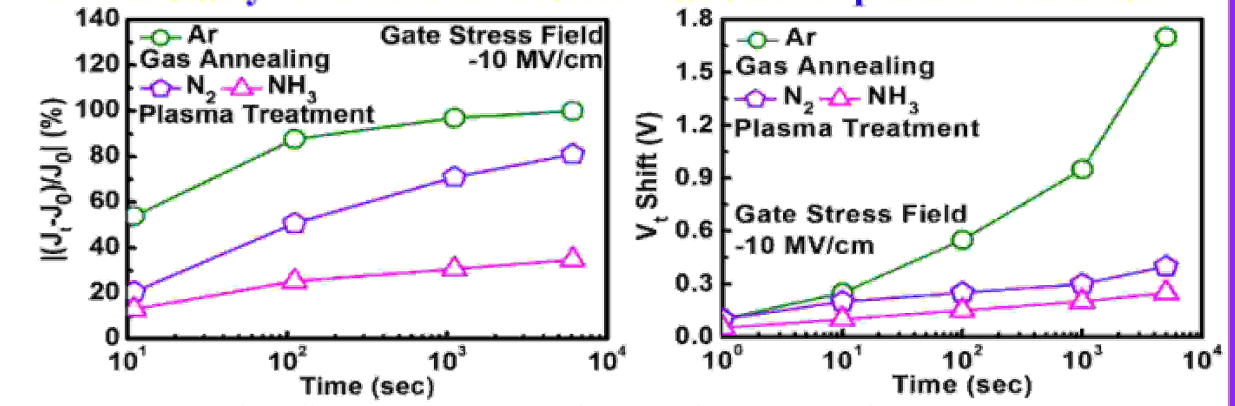

Fig. 11 (a) SILC and (b) V_t shift as a function of stress time under a gate stress field of -10 MV cm^{-1} for devices with different treatments. Additional plasma treatment greatly suppresses the V_t shift.

P-Channel TFT	This Work		2017 [7]	2016 [10]	2015 [9]	2014 [8]	2014 [3]	2013 [2]
Channel Material (Sn %) (thickness)	Poly GeSn (Sn: 5.1 %) (12 nm)		Poly GeSn (Sn: 2 %) (80 nm)	Single GeSn (Sn: 2 %) (80 nm)	Single GeSn (Sn: <3 %) (160 nm)	Poly GeSn (Sn: 3 %) (17.1 nm)	Poly Ge (90 nm)	Poly Ge (20 nm)
Channel Treatment	Ar Gas Annealing	Ar Gas Annealing /NH_3 Plasma	Complete Melting	Local Melting	RTA	Water Laser Annealing	Flash Lamp Annealing	Thermal Annealing
Thermal Process of Channel Treatment	500 °C/30 sec	500 °C/30 sec	> 938 °C/1 sec		880 °C/1 sec	NA	NA	600 °C/5 hr
Gate Dielectric (thickness)	Al_2O_3 (14 nm)		SiO_2 (230 nm)		SiO_2 (NA)	HfAlO (NA)	HfAlO (5 nm)	HfAlO (5.2 nm)
Structure	Planar		Planar		Planar	Tri-Gate	Tri-Gate	Tri-Gate
I_{ON}/I_{OFF} (Gate/Drain Voltage)	1.7×10^4 (V_G = -5 V) (V_D=-0.05 V)	2.8×10^5 (V_G = -5 V) (V_D= -0.05 V)	~10^1 (V_G = -30 V) (V_D= -0.05 V)	3×10^2 (V_G = -30 V) (V_D= -0.05 V)	~2×10^2 (V_G = -100 V) (V_D= -0.5 V)	~10^5 (V_G = -1 V) (V_D= -0.05 V)	< 10^4 (V_G = -2 V) (V_D= -0.05 V)	~10^5 (V_G = -3 V) (V_D= -1 V)
Peak Hole Mobility (cm^2/Vs)	μ_{FE}: 39.3	μ_{FE}:162.2	μ_{FE}: 26	μ_{FE}: 423	μ_{EFF}: 383	μ_{EFF}: 31	μ_{FE}: 115	μ_{EFF}: 24

研究生活與心得

自從來到國立清華大學，感謝巫勇賢教授給予學生的悉心教導以及充沛的資源，讓學生在博士班生涯的路途上可以走得比較順遂，同時能夠獲得這麼豐富的研究成果，以及參加國外研討會所拓展的視野，也要感謝同儕們，在博士班期間給予的鼓勵以及相互切磋，讓學生在半導體的專業部份可以獲得更多的知識，在指導教授以及同儕們的教學相長下，讓我在這崎嶇的道路上走得更加順遂，並迎向未來這美麗的康莊大道；最後非常感謝中技社提供這麼豐厚的研究生獎助學金，使學生不僅獲得實質上的支持，在精神上更是獲得一大鼓勵，在到畢業之前報著感恩的心持續致力於研究上，希望在畢業之後可以發揮學生所長，為了台灣的未來可以回饋於國家及社會。

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