2021「中技社科技獎學金」

2021 CTCI Foundation Science and Technology Scholarship

研究獎學金

Research Scholarship

應用於三維人腦模擬積體電路之高遷移率薄膜電晶體與高可靠度電阻式記憶體

High Mobility TFT and High Reliability RRAM Devices for Three-Dimensional Brain-Mimicking IC

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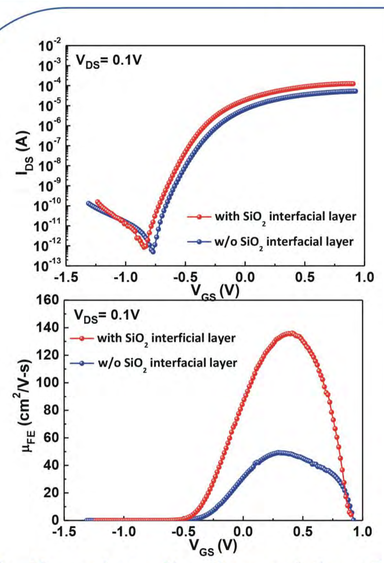
研究重點

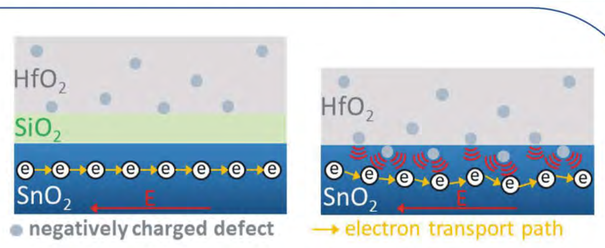
在研究中透過調整電晶體各層薄膜製程方式及界面品質，減少不利於電晶體操作的特性，例如scattering現象，分別在n型、p型電晶體達到高電子及電洞遷移率，藉以應用於高速邏輯運算，有別於傳統CMOS邏輯，薄膜電晶體可以跳脫基板限制，無論要製做在透明玻璃或是可彎曲的材料上都可以彈性應用，擁有更多樣的發展性;電阻式記憶體方面使用離子植入方式降低操作電壓，以達到高操作速度及阻態高穩定性，透過設定不同電壓電流的操作去達到不同阻態，模擬神經網路受到不同刺激會傳遞不同訊息的現象，最終欲將兩種研究做結合，透過適當排列及多層3D堆疊，期望未來能做到人腦神經元模擬IC，同時高速處理大量運算及傳遞訊號。

研究成果

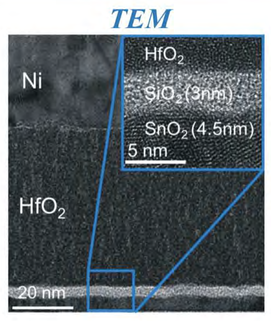
N type Thin-Film Transistor (n-TFT)

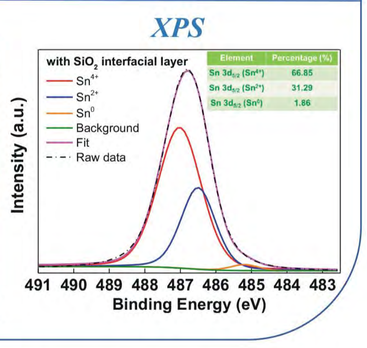


I_{DS}-V_{GS} and μ_{FE}-V_{GS} characteristics of the top-gate SnO_2 TFTs with and without an SiO_2 interfacial layer.

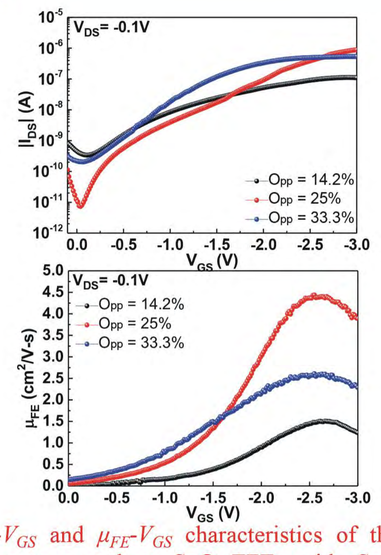


The schematic diagrams for electron transport in SnO_2 with and without an SiO_2 interfacial layer.

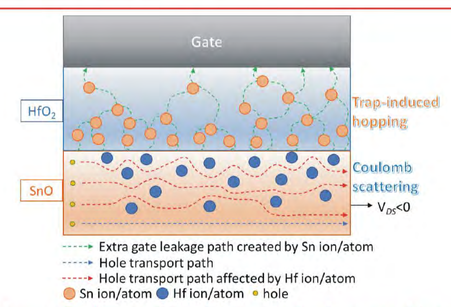




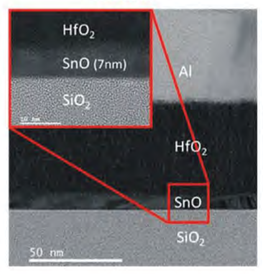
P type Thin-Film Transistor (p-TFT)

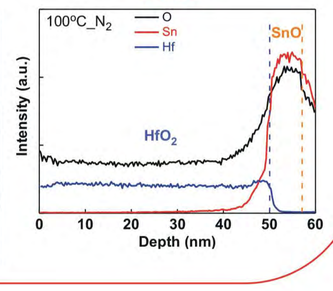


I_{DS}-V_{GS} and μ_{FE}-V_{GS} characteristics of the top-gate nanosheet SnO TFTs with SnO channel deposited at different O_{pp} conditions.

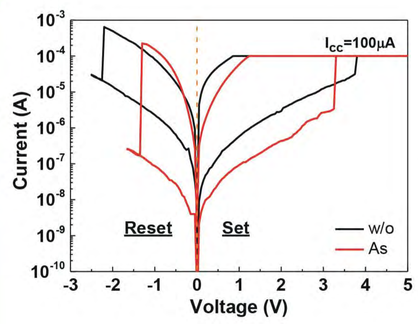


Schematic diagram to show gate leakage and inter-diffusion of top-gate SnO TFT device annealed at 200 ℃.

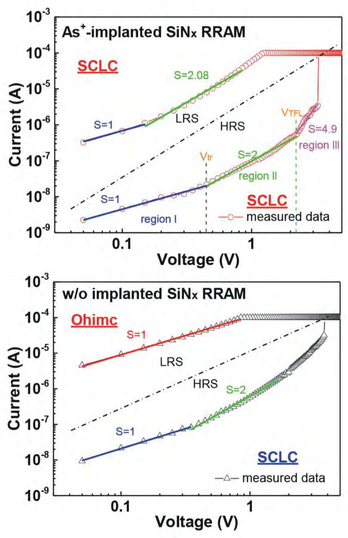


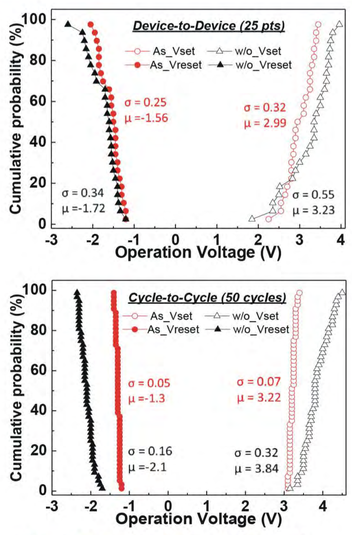


Resistive Random Access Memory (RRAM)

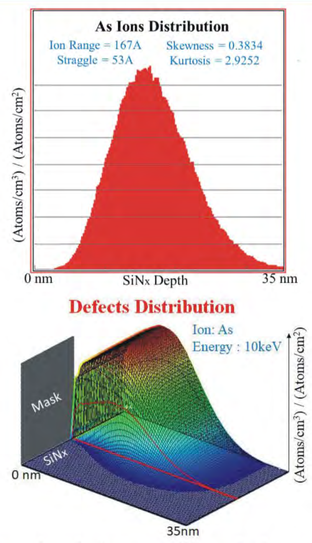


The I–V characteristics and analyzed I-V curves at the set–reset process of the As^+-implanted and nonimplanted SiN_x RRAM.

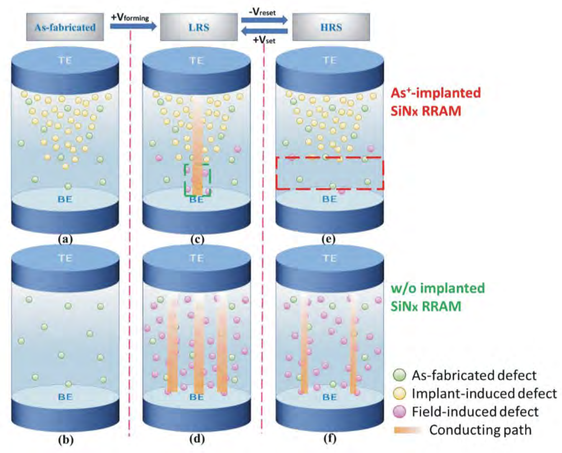




The D2D and C2C of V_{set}–V_{reset} distribution of As^+- and without implanted SiN_x RRAM devices.



The simulation results of the As atoms and 3D defect distribution of the As^+-implanted SiN_x layer.



The schematic diagram of defect distribution and potential resistance switching characteristics in As^+-implanted and nonimplanted SiN_x RRAM devices.

研究生活與心得

在陽明交通大學就讀期間，從懵懂的研究生慢慢學習變成現在能獨立做研究，且有餘力指導碩班學弟妹的博士班學長，從懷疑自己能力到一路通過博士資格考且發表數篇國際論文，過程中雖然到許多挫折，但透過不斷從錯誤中學習，這幾年的努力得到了很大的回報，這一切對我來說意義非凡，要特別感謝我的指導教授荊鳳德老師對我的循循善誘且給予我研究上很大的空間，讓我能在做研究的路上能盡情發揮，在與俄羅斯科學院的合作中學習到許多分析數據的技巧，與不同領域的人接觸讓我眼界更廣闊，謝謝家人的全力支持，使我能無後顧之憂的攻讀博士學位，感謝中技社科技獎學金及評審委員的青睞，期許自己未來能更進步，對科技產業有所貢獻。