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Research Scholarship for International Graduate Students

Gradual, Synaptic and Optical Memristors

Aftab Saleem (Ph.D. 4th)[1], Tseung-Yuen Tseng(Professor)(Advisor)[2]

國立陽明交通大學 NATIONAL YANG MING CHIAO TUNG UNIVERSITY

1. Department of Electrical Engineering and Computer Science, National Yang Ming Chiao Tung University, Taiwan
2. Institute of Electronics, National Yang Ming Chiao Tung University, Taiwan

Abstract

In recent times, with the evolution of machine learning and artificial intelligence the von-Neumann architecture is reaching a bottleneck and new emerging technologies are showing promising features to take its place. Memristors are one of these emerging technologies. Memristors using transition metal oxides as their switching layers are highly stable, fast and scalable. These attributes make them a suitable option for parallel computing. For machine learning applications or to mimic neuromorphic functions of brain synaptic memories should be fabricated. Synaptic memories provide gradual conductance change and make multi-level cell characteristic possible. For getting gradual conductance change in memristors different techniques are being used like annealing, ion implantation and barrier layer insertion. In MLC by changing the input schemes we can tune the device at several different conductance states. Apart from synaptic function in memristors, these devices can also be fabricated on polymers for green and wearable electronics. The new advancement in this field has drifted towards optical memristor devices in which light illumination is used to change the conductance of device. For illuminations of devices different wavelength lasers are being used with different illuminating time and different illuminating intensities

Results

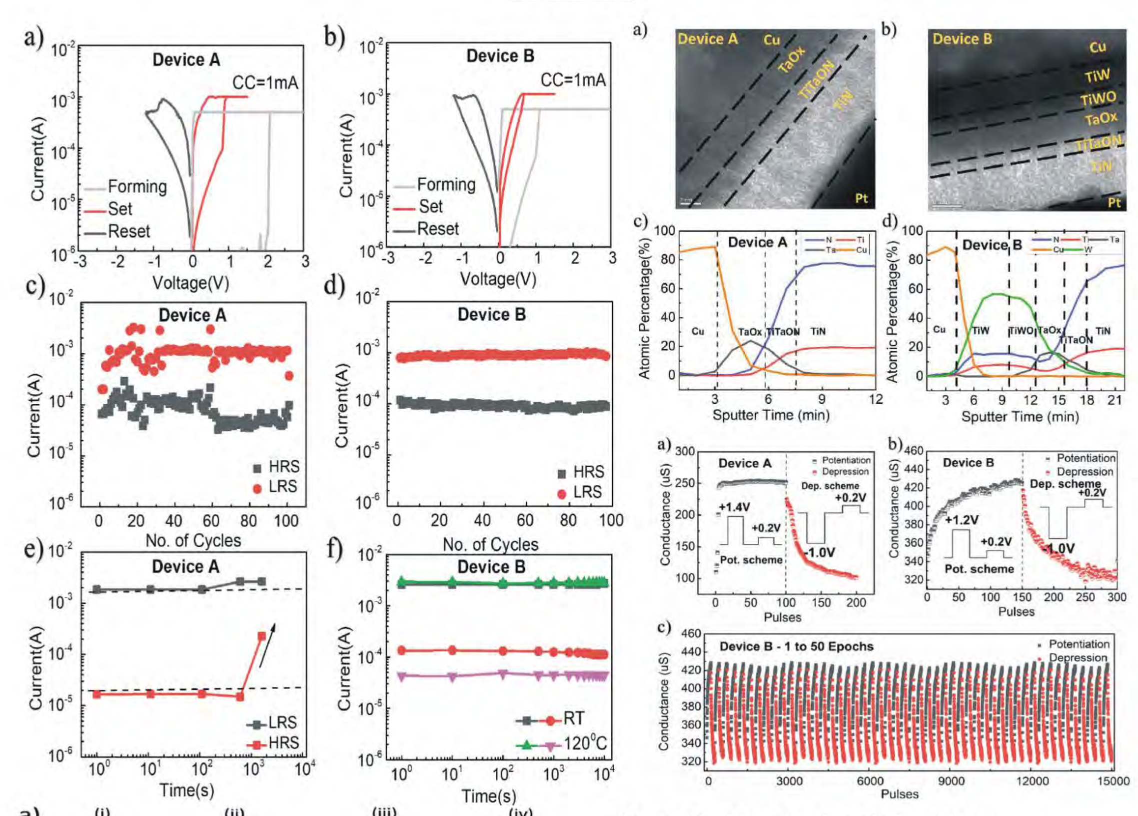

Figure 1. Electrical and chemical characterization of device Potentiation and Depression cycles with high endurance

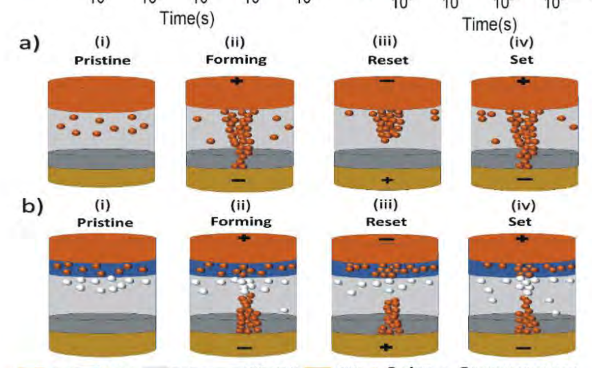

Figure 2. Proposed Switching mechanism for Device without barrier layer and with barrier Layer, respectively.

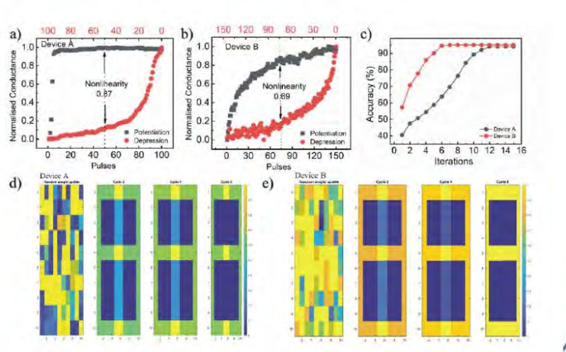

Figure 3. Non-linearity coefficient calculation with HNN pattern recognition accuracy curve.

Explanation

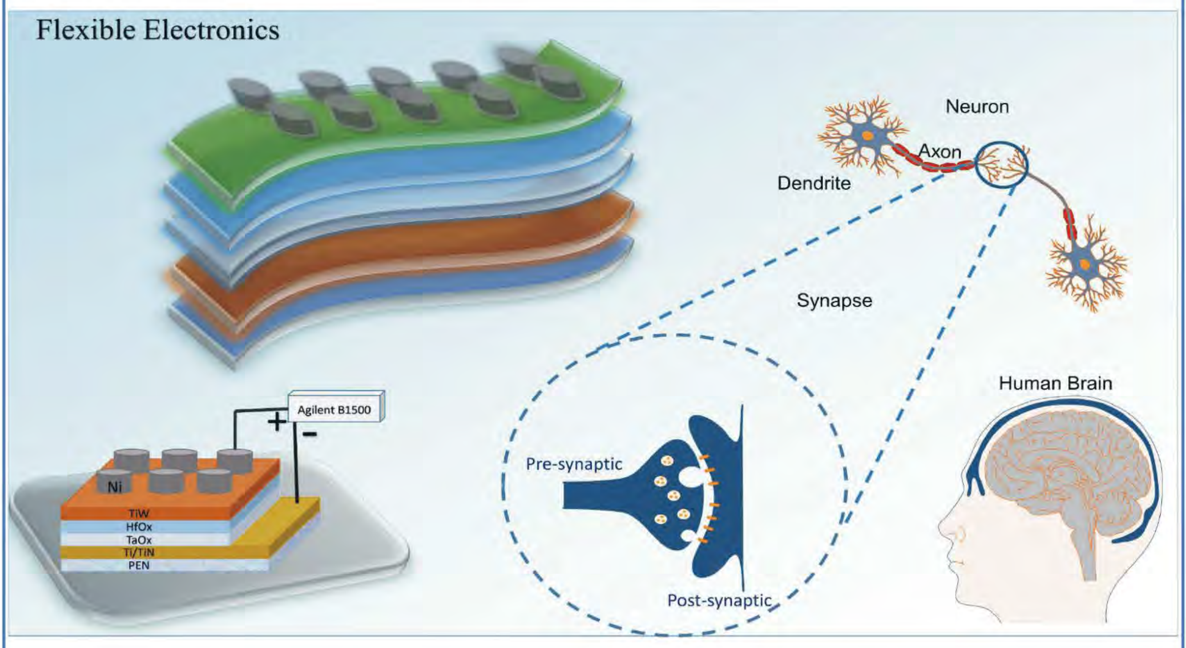

Figure 4. Flexible electronics schematics along with visual representation of a neuron having pre-synapse and post-synapse .

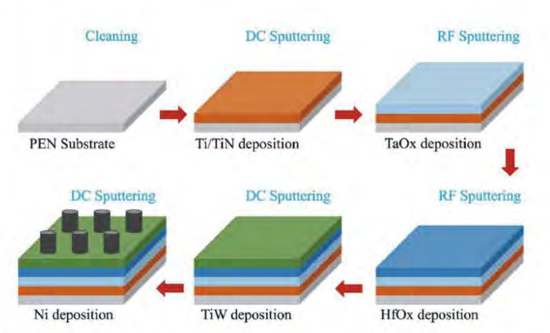

Figure 5. Fabrication process for flexible memristors from cleaning to full device stack.

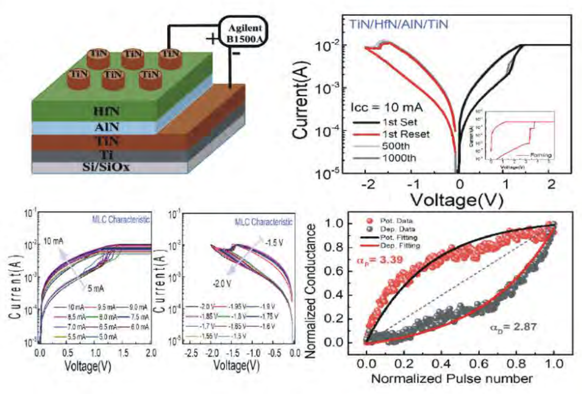

Figure 6. A nitride based memristor showing multi-level cell characteristics and having low co-efficient of non-linearity.

Discussions

Transition Metal Oxides such as HfO_2, SnO_2, ZnO, NiO, WO_x, TiO and ZrO_2 have been studied by researchers in the past decade due to their good memristive capabilities. Mostly, memristors with digital switching were studied for their highly stable data and good switching speed. However, analog switching is desirable with electrical pulses to mimic synaptic function for neuromorphic computing. In recent times, TaOx has shown good performance and high reliability with synaptic application by utilizing different engineering techniques to achieve analog switching. Though, fabricating flexible analog memristor with good performance and high reliability still poses great challenges, in order to launch commercial devices for wearable electronics.[20] For high density data storage, realization of multilevel cell characteristic (MLC) is an important aspect which has been extensively addressed over past few years. The randomly grown filaments in switching layers hinder MLC capability of device. Therefore, different interfacial engineering techniques such as doping of impurity, multiple temperature annealing and insertion of barrier layer or modulation layer were applied to confine the filament area in order to achieve stable MLC capability. Moreover, mostly memristors tend to degrade their storage capabilities under humid and varying temperature environment. Considerable amount of research is inclined towards this to mitigate these issues and make devices favorable for wearable electronics.

Fabrication Process

A 20-nm-thick TiN bottom electrode (BE) was deposited onto a Pt/Ti/SiO2/Si substrate by plasma-enhanced atomic layer deposition. The use of a thin layer of Pt benefits to reduce the sheet resistance of the TiN electrode. A 10 nm TaOx layer was deposited using the RF sputtering technique. The sputtering power, gas flow ratio (Ar/O2), and working pressure were 100W, 2/1, and 10 mTorr, respectively. A 100-nm-thick Cu top electrode (TE) with a diameter of 150 lm was patterned using a shadow mask. For making a Cu/TiW/TaOx/TiN stack, a 20-nm-thick TiW layer was deposited by DC sputtering. All layers were deposited at room temperature. The device fabricated without the insertion of TiW as a barrier layer is used as the reference or control sample and is denoted as Device A, while the device made with BL is denoted as Device B. Switching and synaptic characteristics were measured using an Agilent B1500A probe station. A voltage bias was applied at the Cu top electrode, and the TiN bottom electrode was kept ground. A compliance current (Icc) during positive bias was used to prevent device breakdown. The film structure of the devices was investigated using a transmission electron microscope (TEM, JEOL 2100FX). The element profile of the film and the oxygen defect distributions of the oxide layers were investigated by x-ray photoelectron spectroscopy (XPS, PHI Quantera SXM).

Towards Optical Memristor

In order to achieve ORRAM structure, transition metal oxide layers suitable for available wavelengths are being optimized. The goal is to fabricate an optical memory device which is both capable of electrical /optical switching and neuromorphic computing.

Publications

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[4] Sailesh Rajasekaran et al. **Aftab Saleem,** and Tseung-Yuen Tseng.
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Book Chapter:

[5] "Practical Approach to Induce Analog Switching Behavior in Memristive Devices: Digital-to-Analog Transformation"
Mangasa Simanjuntak, Firman et al., **Saleem, Aftab** (10.5772/intechopen.98607)

Submitted

[6] "Oxygen Vacancy Transition in HfOx Based Flexible, Robust and Synaptic Bi-layer Memristor for Neuromorphic and Wearable Applications"
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[7] "Highly Efficient Invisible TaO_x/ZTO Bilayer Memristor for Neuromorphic Computing and Image Sensing" Dayanand Kumar*, **Aftab Saleem** et al. [ACS Nano]

[8] "Improved Synaptic Characteristics in Bilayer Memristor by Post-Oxide Deposition Annealing for Pattern Recognition"
Dayanand Kumar, **Aftab Saleem** et al. Tseung Yuen Tseng [IEEE VLSI]

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Contact: afymalik@yahoo.com

Phone # +886928495942

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