2022「中技社科技獎學金」

2022 CTCI Foundation Science and Technology Scholarship

研究獎學金

Research Scholarship

具分散式相關電壓位移與多重參考電壓嵌入式比較器之類比數位轉換器

Analog-to-Digital Converters with Distributed Correlated Level Shifting and Multiple-Reference-Embedded Comparator

國立成功大學　電機系博士班六年級　王家慶

指導教授：郭泰豪 特聘教授

MSIC Lab Mixed Signal IC Laboratory

NATIONAL CHENG KUNG UNIVERSITY 1931

Motivation:

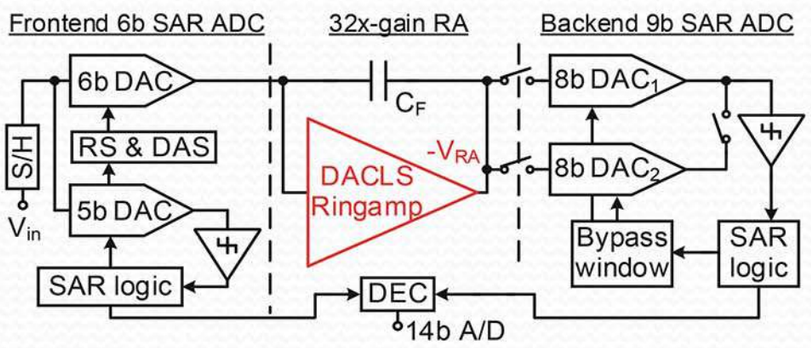
To fulfill upcoming communication specifications, a high-performance analog-to-digital converter (ADC) becomes essential for a mobile system. In addition, for IoT devices, the power consumption and the area are also significant so as to achieve a long battery life and a low chip cost, respectively. Thus, this research proposed several ADC design techniques for both high-resolution and high-speed applications.

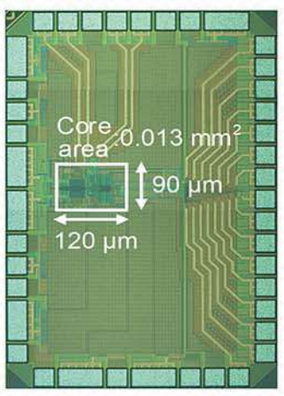
Research Highlights:

High-resolution pipelined-SAR ADCs

IEEE ISSCC & IEEE JSSC (2020, 2022)

1. This 28nm 14b 130MS/s ADC is the first to break the Walden FoM barrier of 2fJ/conv. for >40MS/s ADCs.
2. The proposed distributed averaging correlated level shifting (DACLS) ringamp accomplishes the reduction of finite opamp gain (A) error and results in the equivalent residue amplifier (RA) open-loop gain approaching $O(A^3)$.
3. Under the 85-dB equivalent RA open-loop gain target in this work, the RA bandwidth of the proposed DACLS ringamp is improved by over 2.2x compared to prior arts.
4. The proposed latency-reduced SAR logic and the customized bypass-window backend improves the SAR bit-cycling speed by ~30% and reduces the backend ADC power consumption by ~30%, respectively.

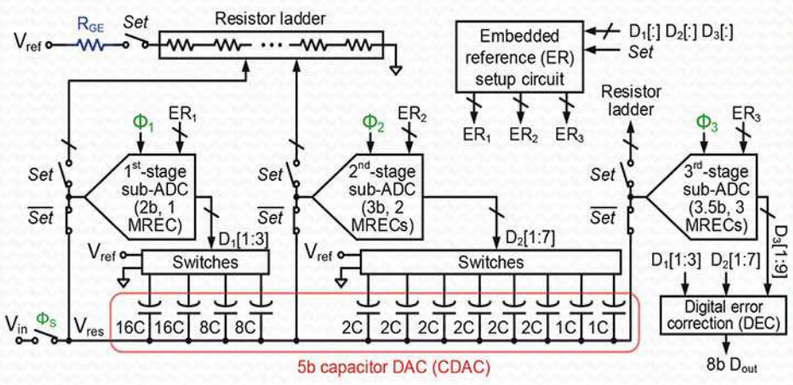


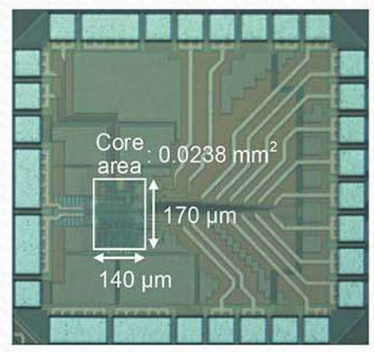


High-speed subranging ADCs

IEEE VLSIC (2022) & *IEEE ISSCC* (2023)

1. This 28nm 8b 2.7GS/s ADC achieves the highest sampling rate among ≥6b single-channel ADCs and a 6.9-fJ/conv. Walden FoM advancing prior arts by ~30%.
2. The proposed multiple-reference-embedded comparator (MREC) accomplishes multiple comparisons and multiple embedded references (ERs) by a single comparator and results in a ~50% power reduction.
3. A rotational calibration scheme is implemented so as to guarantee the accuracy of all ER voltages in an MREC.
4. The proposed kickback compensator retains the nominal common-mode voltage of the residue so as to diminish the kickback-induced dynamic comparator offset in sub-ADCs.





得獎感言:

非常榮幸也感謝能被中技社授予這個獎項，這也是對本團隊成果的肯定。首先，我必須要感謝我的指導教授郭泰豪博士。無論是老師提供的平台以及資源，還是老師對我的不吝指導與包容，沒有老師的幫助，就沒有學生我今日的成果。其次，我也感謝MSIC實驗室前輩的指導以及同學的幫助。當然，我也十分感謝我的家人，在我博士班期間對我的一切支持。最後，我希望能用晚清名臣曾文正公的一句話來繼續砥礪自己並與大家共勉，「堅其志，苦其心，勞其力，事無大小，必有所成」。

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